AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at line 19, page 1 as follows.

Wire bonding has been the predominatent structure for ~~connecting to a~~connections to semiconductor interconnects and it is used in a significant share of all leaded packages. Briefly, a wire bonding is a low-temperature welding process. As an alternative technique to welding, conventional wire bonding uses ultrasonic energy that is applied through a bonding tool (called a capillary or wedge) to a wire and a bond site. This energy increases the dislocation density of the wire and bond site, lowering flow stress and modulus of elasticity while increasing the rate of diffusion. This causes the material to deform easily at much lower stresses than would otherwise be required.

Please amend the paragraph beginning at line 11, page 2 as follows.

As one example of known wire bonding technology, an advanced copper interconnect system (U.S. Patent No. 5,785,236 entitled "Advanced Copper Interconnect System Compatible With Existing Bonding Technology") is illustrated in Figure 1. A gold wire bonding (gold wire not shown) is carried out by applying an aluminum pad 13 over ~~a~~ copper interconnects 12 and a dielectric 11. These are deposited on a silicon wafer 10, through an opening formed on a passivation layer 14. As shown in Figure 1, this additional cap metallization (aluminum pad 13) process enables electrical connections to be formed between the gold wire (not shown) and the copper interconnects 12 through the aluminum pad 13. The system enables the conventional wire bonding techniques to be employed on the copper interconnects 12. However, the additional step of forming the aluminum pad 13 involves a complicated semiconductor fabrication process such as a lithography step and a chemical etching step, which increases manufacturing cost.

Please amend the paragraph beginning at line 20, page 3 as follows.

One aspect of the present invention is to provide a process of forming metal surfaces on a bare metal chip. The metal chip includes metal interconnects formed on a semiconductor substrate and at least a portion of the metal interconnects is exposed to the environment. The

process comprises applying a noble metal on the portion of the exposed metal interconnects and performing a chemical process that causes a layer of the noble metal to convert to a bondable layer compatible with a wire bonding. The process also comprises bonding a metal wire to the bondable layer.

Please amend the paragraph beginning at line 12, page 5 as follows.

This invention relates to a process of forming metal surfaces in a semiconductor device with metal interconnects such as copper (Cu) interconnects, copper alloy, other possible combinations of copper alloys, and other metal interconnects, using conventional Au and Al wire bond tools. The invention may be applied to metallization which is incompatible with conventional wire bonding. By using a suitable low cost intermediate process, according to this invention, a bond pad, which is a part of the Cu interconnect and exposed to the environment, is converted to a bondable layer that can be bonded to a conventional metal wire, such as an Au or Al wire (not shown).

Please amend the paragraph beginning at line 14, page 10 as follows.

Furthermore, the process according to the invention can also be additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out. The structure includes any shape or form (e.g. thick, thin, round, square, with via, etc.) ~~that~~on which ~~a~~ the bond pad can form ~~tae~~. Also, it is not strictly restricted to conventional bond pads alone. In addition, the structure includes any device surface on which the process provided by the process of the invention is applied.

Please amend the paragraph beginning at line 28, page 10 as follows.

Figures 10a-11 are drawings for comparing the prior art and the present invention. Figure 10a illustrates a conventional bare Cu chip. Figure 10b illustrates one of the prior wire bonding techniques that uses Al cap metallization. Figure 11 illustrates a wire bonding technique according to the present invention.

Please amend the paragraph beginning at line 1, page 11 as follows.

Figure 10a is substantially the same as Figure 4a. A silicon wafer 100 and an oxide/dielectric layer 102 in Figure 10a corresponds to a silicon layer 40 and a dielectric 41 in Figure 4a. A Cu metallization 101 in Figure 10a corresponds to the Cu interconnects 42 shown in Figure 4a. Reference numeral 103 represents a passivation layer.

Please amend the paragraph beginning at line 10, page 11 as follows.

Figure 11 illustrates one embodiment of the present invention. A bondable layer 111 formed by the process of the present invention is compatible with conventional wire bonding technique, such as an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof. The main ~~diffenrece~~difference between the process of Figure 11 and the process of Figure 10b is that the process of Figure 11 uses a simple chemical process to form the bondable layer 111, while the process of Figure 10b uses a complicated semiconductor fabrication process to form the Al cap metallization 104.